इंटरनेट मानक

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Mazdoor Kisan Shakti Sangathan
"The Right to Information, The Right to Live"

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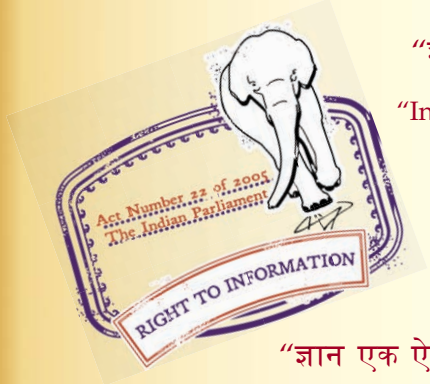
Jawaharlal Nehru
"Step Out From the Old to the New"

IS 11845-1 (1994): Fluid logic circuits for fluid power systems, Part 1: symbols for binary logic and related functions [PGD 16: Fluid Power]



"ज्ञान से एक नये भारत का निर्माण"
Satyanarayan Gangaram Pitroda
"Invent a New India Using Knowledge"

"ज्ञान एक ऐसा खजाना है जो कभी चुराया नहीं जा सकता है"
Bhartṛhari—Nītiśatakam
"Knowledge is such a treasure which cannot be stolen"

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IS 11845 (Part 1) : 1994
ISO 5784-1 : 1988

(Reaffirmed 1999)

भारतीय मानक

तरल पावर तंत्रों के लिए तरल तर्क परिपथ

भाग 1 द्विआधारी तर्क और संबोधित कार्यों के लिए प्रतीक

(पहला पुनरीक्षण)

Indian Standard

FLUID LOGIC CIRCUITS FOR FLUID POWER SYSTEMS

PART 1 SYMBOLS FOR BINARY LOGIC AND RELATED FUNCTIONS

(First Revision)

ISO Title : Fluid power systems and components — Fluid logic circuits: Part 1 Symbols for binary logic and related functions

UDC 621·22:744·423 : 003·62

BUREAU OF INDIAN STANDARDS
MANAK BHAVAN, 9 BAHADUR SHAH ZAFAR MARG
NEW DELHI 110 002

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Price Group 9

NATIONAL FOREWORD

This Indian Standard (Part 1) (First Revision) which is identical with ISO 5784-1:1988 'Fluid power systems and components — Fluid logic circuits — Part 1: Symbols for binary logic and related functions', issued by the International Organization for Standardization (ISO), was adopted by the Bureau of Indian Standards on the recommendations of the Basic Fluid Power Sectional Committee and approved by the Production Engineering Division Council.

This standard was first issued in 1986 based on ISODIS 5784/1. Consequent upon the publication of ISO 5784-1 : 1988, this standard has been revised by adopting ISO 5784-1:1988, to bring it in line with ISO standard. This standard have been formulated into three parts. The other two parts are as follows:

a) IS 11845 (Part 2) 1994/ISO 5784-2:1989 Fluid logic circuits for fluid power systems : Part 2 Symbols for supply and exhausts as related to logic symbols.

b) IS 11845 (Part 3) 1994/ISO 5784-3:1989 Fluid logic circuits for fluid power systems : Part 3 Symbols for logic sequences and related functions.

The text of the ISO standard has been approved as suitable for publication as Indian Standard without deviations. Certain conventions are, however, not identical to those used in Indian Standards. Attention is particularly drawn to the following:

a) Comma (,) has been used as a decimal marker in the International Standard while in Indian standards, the current practice is to use a point (.) as a decimal marker.

b) Wherever the words 'International Standard' appear referring to this standard, they should be read as 'Indian Standard'.

In the adopted standard, reference appears to certain International Standards for which Indian Standards also exist. The corresponding Indian Standards which are to be substituted in their place are listed below along with their degree of equivalence for the editions indicated:

International Standards	*Corresponding Indian Standards*	*Degree of Equivalence*
ISO 1219:1976	IS 7513:1974 Graphical symbols for fluid power systems	Technically equivalent
ISO 5598:1985	IS 10416:1992 Fluid power systems and components—Vocabulary	Identical

The concerned technical committee has reviewed the provision of IEC Publication 617-12 Graphical symbols for diagrams: Part 12 Binary logic elements referred in this adopted standard to use in conjunction with this standard.

Indian Standard

FLUID LOGIC CIRCUITS FOR FLUID POWER SYSTEMS

PART 1 SYMBOLS FOR BINARY LOGIC AND RELATED FUNCTIONS

(First Revision)

0 Introduction

0.1 In fluid power systems, power is transmitted and controlled through a fluid (liquid or gas) under pressure within a circuit.

Graphical symbols are used in diagrams of hydraulic and pneumatic equipment and accessories for fluid power transmission.

0.2 ISO 5784 on symbols for fluid logic circuits comprises the following three parts:

Part 1: Symbols for binary logic and related functions.

Part 2: Symbols for supply and exhausts as related to logic symbols.

Part 3: Symbols for logic sequencers and related functions.

1 Scope and field of application

This part of ISO 5784 defines graphical symbols for binary logic and related functions and gives some rules concerning their use in circuit diagrams.

Symbols given in this part of ISO 5784 shall be used for all documents and circuit diagrams concerning logic and related functions for data processing, especially in fluid logic circuits.

2 References

ISO 1219, *Fluid power systems and components — Graphic symbols.* [1)]

ISO 5598, *Fluid power systems and components — Vocabulary.*

IEC Publication 617-12, *Graphical symbols for diagrams — Part 12: Binary logic elements.*

3 Definitions

For the purposes of this part of ISO 5784, the definitions given in ISO 5598 apply.

4 General

The two values of a binary digital variable are assigned logic states which may be represented by any two arbitrary symbols. It has become usual practice to use the symbols 0 and 1 for this purpose.

In fluid logic applications the logic states represent two different pressure levels. Normally the higher pressure level represents the logic state 1 (positive logic).

5 Composition of the symbols and rules for their use

5.1 General rules

The following rules are applicable to all the symbols presented in this part of ISO 5784.

The form A symbols in this part of ISO 5784 are in accordance with IEC Publication 617-12 and are to be preferred; the form B symbols, although currently used, are not preferred for future use.

This part of ISO 5784 gives the most currently used logic functions and shows also how to apply these rules. Subject to these rules any other symbols may be developed.

NOTES

1 The following examples make use of the letters X, Y, Z, S... a, b, c, etc., to define logic equations. The convention is used for convenience only and should not be taken as part of the requirements laid down in this part of ISO 5784.

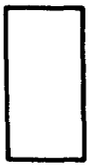
2 The addition of truth tables and Boolean equations are meant as explanations; they are not part of the requirements laid down in this part of ISO 5784.

1) The cross-reference to item 8.1.1 in ISO 1219 applies to the first edition published in 1976.

5.2 Composition of the symbols

A symbol comprises the following parts:

a) An outline

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 200-05/1		Logic element: General symbol The choice of form A or B is left to the user but reference shall be made to 5.1. However in any given circuit diagram, only one form (either A or B) shall be used. NOTE — The aspect ratio is arbitrary.	
5 200-06/1			

b) A qualifying symbol denoting the logic function

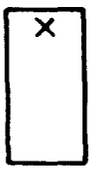
This is a symbol which specifies the required logic operation. In certain cases, this symbol may be accompanied by numerical values necessary to define the function of the element.

This symbol and/or these numerical values are drawn usually inside the outline.

c) Indicators for inputs and outputs

Each of these indicators is related to the input or the output against which it appears. The indicators shall be positioned as indicated in clause 5.3.

5.3 Position of the qualifying symbol for the logic function

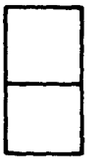
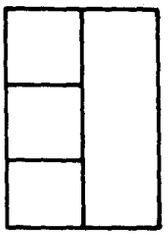
Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 300-05/1		The qualifying symbol for the function or the numerical values is (are) located in the top centre of the outline or in the centre (form A) or in the centre of the outline (form B).	

5.4 Additional information

Any kind of additional information, e.g. type, function or location of the element, shall be written outside the outline of the symbol, below or following the qualifying symbol.

1) This form is not preferred for future use (see 5.1).

5.5 Combination of symbols

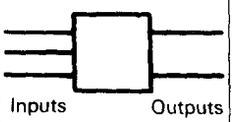
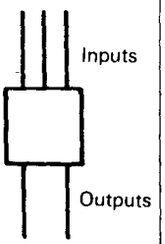
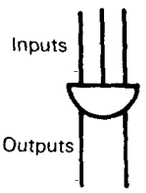
Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 500-05/1		Separated symbols shall be used in logic circuit diagrams; however, to reduce space required on the diagram, symbols for basic operations may be joined together but the following rules shall then be complied with: a) there is no logic connection when the half-circles are tangents (form B) or the common line to two symbols is in the direction of information flow (form A); b) there is single logic connection, without logic inversion, when the common line to two symbols is perpendicular to the direction of information flow.	
5 500-06/1			

5.6 Direction of information flow

Code number	Graphical symbol Forms A and B	Description
5 600-05/1		In principle, the information flow is directed from left to right or from top to bottom. If this is not possible and the direction of information flow is not obvious, lines carrying information with arrow heads may be marked which shall not be located adjacent to the logic symbol at inputs and outputs.

5.7 Inputs and outputs

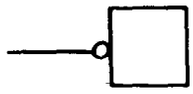
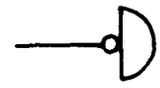
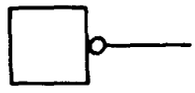
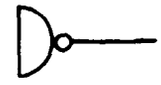
5.7.1 Input and output connections to the symbol

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 710-05/1		The inputs and outputs are located on opposite sides of the symbol.	
5 710-06/1		A logic symbol may have any number of inputs and outputs providing the symbol definition requirements are met.	

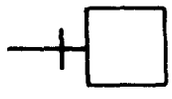
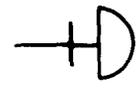
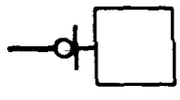
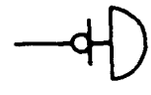
1) This form is not preferred for future use (see 5.1).

5.7.2 Negation

The state of the logic variable at an input or output is reversed if the logic negation indicator is applied.

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 720-05/1		Logic negation indicator (complement)	
5 720-10/1		Negated input	
5 720-15/1		Negated output NOTE — The line of input or output may be drawn through the circle.	

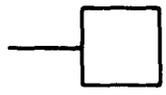
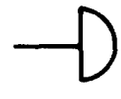
5.7.3 Inhibiting and negated inhibiting inputs

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 730-05/1		Inhibiting input: a) an inhibiting input of a digital element standing at its defined 1-state prevents the output variable of that element from standing at its defined 1-state (or its 0-state if the output is negated) whatever the value of the other input variables; b) when the inhibiting input stands at its 0-state the qualifying symbol of the element applies to those inputs which are neither inhibiting inputs nor negated inhibiting inputs.	
5 730-10/1		Negated inhibiting input: a) a negated inhibiting input of a digital element standing at its 0-state prevents the output variable of that element from standing at its defined 1-state (or its 0-state if the output is negated) whatever the value of the other input variables; b) when the negated inhibiting input stands at its defined 1-state the qualifying symbol of the element applies to those inputs which are neither inhibiting inputs nor negated inhibiting inputs.	

5.7.4 Static and dynamic inputs

5.7.4.1 Static input

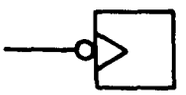
A static input is one such that 1-state is defined as the presence of a particular digital level, and the 0-state as the presence of the other logic level.

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 741-05/1		Static input	

1) This form is not preferred for future use (see 5.1).

5.7.4.2 Dynamic input

A dynamic input is one such that the 1-state is defined as the transition from a particular digital level to the other digital level and not by the presence of one of these logic levels.

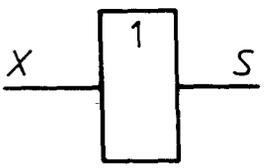
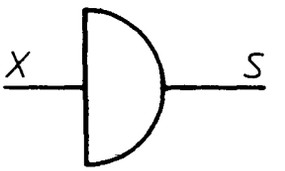
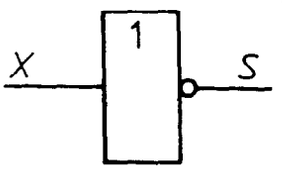
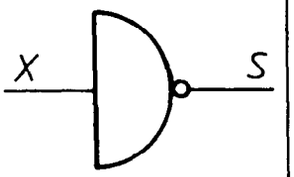
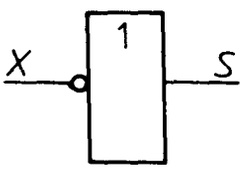
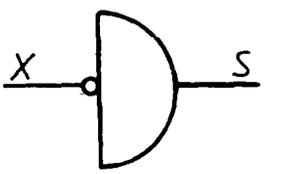
Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 742-05/1		Dynamic input for which the dynamic 1-state is defined by the transition from the static 0-state to the static 1-state.	
5 742-10/1		Dynamic input for which the dynamic 1-state is defined by the transition from the static 1-state to the static 0-state.	

6 Combinative functions

6.1 Basic rule for the composition of the symbol

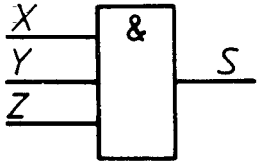
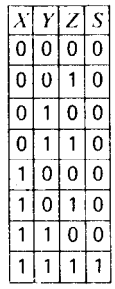
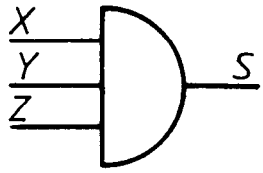
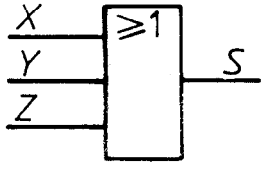
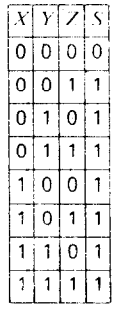
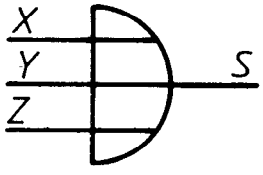
The qualifying symbol indicates the number of inputs which shall necessarily assume the defined 1-state so as to cause the output to assume its defined 1-state provided that the output is not negated.

6.2 Elementary combinative functions

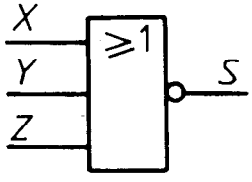
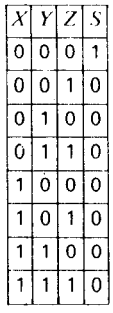
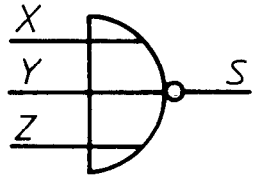
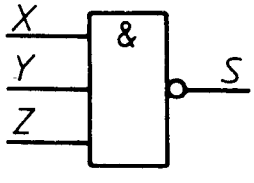
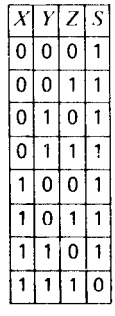
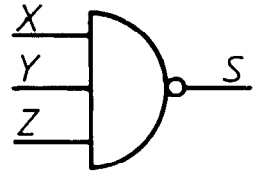
Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
6 200-05/1		YES function X | S 0 | 0 1 | 1 The output will stand at its defined 1-state if, and only if, the input stands at its defined 1-state. $S = X$	
6 200-10/1		NO function The output will stand at its 0-state if, and only if, the input stands at its defined 1-state.	
6 200-11/1		X | S 0 | 1 1 | 0 $S = \overline{X}$	

1) This form is not preferred for future use (see 5.1).

6.2 Elementary combinative functions (*concluded*)

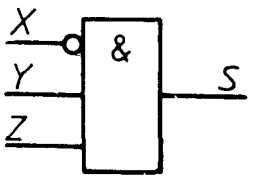
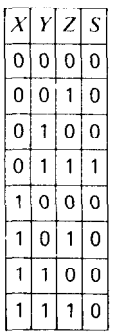
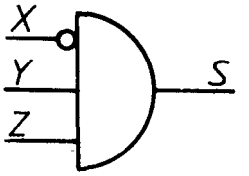
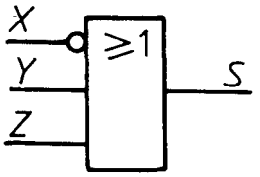
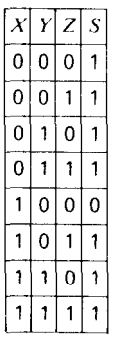
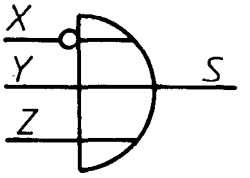
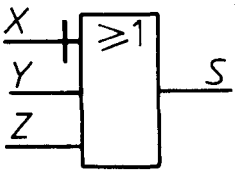
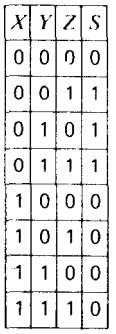
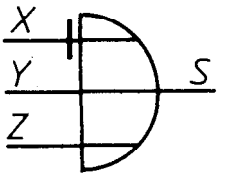
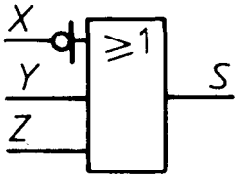
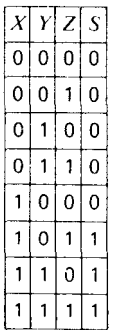
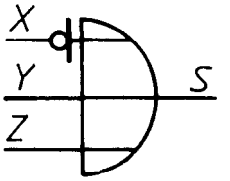
Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
6 200-15/1		 AND function The output will stand at its defined 1-state if, and only if, all of the inputs stand at their defined 1-states. $S = X\,Y\,Z$	
6 200-20/1		 OR function The output will stand at its defined 1-state if, and only if, one or more of its inputs stand at their defined 1-states. $S = X + Y + Z$ NOTE – "≥ 1" may be replaced by "1" if no ambiguity arises.	

6.3 Derived combinative functions – Examples

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
6 300-05/1		 NOR function, i.e. OR function with negated output The output will stand at its 0-state if, and only if, at least one input stands at its defined 1-state. $S = \overline{X + Y + Z}$	
6 300-10/1		 NAND function, i.e. AND function with negated output The output will stand at its 0-state if, and only if, all inputs stand at their defined 1-states. $S = \overline{X\,Y\,Z}$	

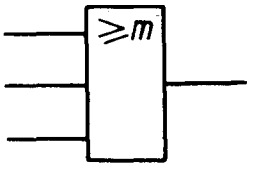
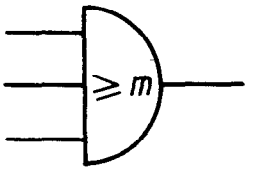
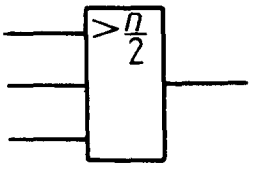
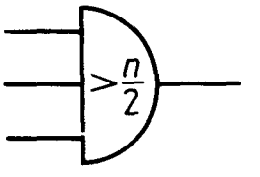
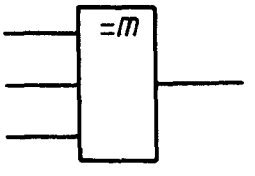
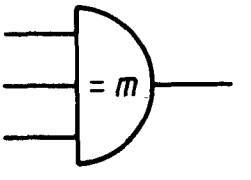
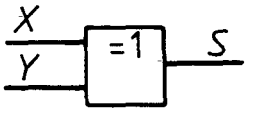
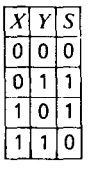
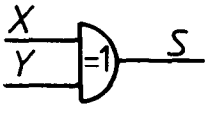
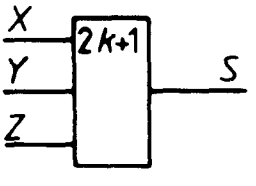
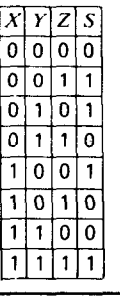
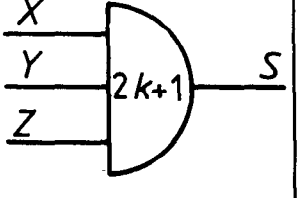
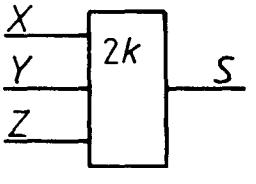
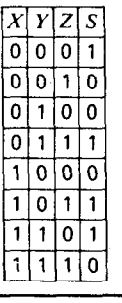
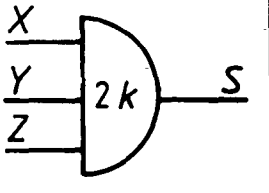
1) This form is not preferred for future use (see 5.1).

6.3 Derived combinative functions — Examples (*concluded*)

Code number	Graphical symbol Form A	Description	Graphical symbol Form B[1]
6 300-15/1		 AND function with one or more negated input(s) The output will stand at its defined 1-state if, and only if, all non-negated inputs stand at their defined 1-states and all negated inputs stand at their 0-states. $S = \overline{X}\,Y\,Z$	
6 300-20/1		 OR function with one or more negated input(s) The output will stand at its defined 1-state if, and only if, one or more non-negated input(s) stand at their defined 1-states and/or one or more negated inputs stand at their 0-states. $S = \overline{X} + Y + Z$	
6 300-25/1		 OR function with one inhibiting input The output will stand at its defined 1-state if, and only if, one or more non-inhibiting input(s) stand at their defined 1-states and the inhibiting input stands at its 0-state. $S = \overline{X}\,(Y + Z)$	
6 300-30/1		 OR function with one negated inhibiting input The output will stand at its defined 1-state if, and only if, one or more non-negated inhibiting input(s) stand at their defined 1-states and the negated inhibiting input stands at its 1-state. $S = X\,(Y + Z)$	

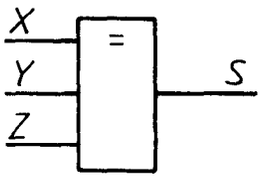
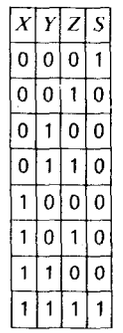
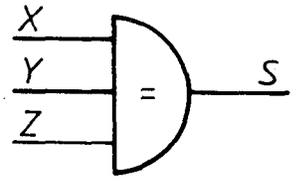
1) This form is not preferred for future use (see 5.1).

6.4 Complex combinative functions

Code number	Graphical symbol Form A	Description	Graphical symbol Form B[1]
6 400-05/1		Logic threshold function The output will stand at its defined 1-state if, and only if, the number of inputs which stand at their defined 1-states reaches or exceeds the number (m) specified in the qualifying symbol. NOTE – m shall always be smaller than the number (n) of inputs.	
6 400-10/1		Majority function The output will stand at its defined 1-state if, and only if, the majority of inputs stand at their defined 1-states.	
6 400-15/1		m and only m function The output will stand at its defined 1-state if m, and only m, of its n inputs stand at their defined 1-states. NOTE – m shall always be smaller than the number (n) of inputs.	
6 400-20/1		 Exclusive OR function The output will stand at its defined 1-state if one, and only one, of the inputs stands at its defined 1-state.	
6 400-25/1		 Addition modulo 2 (parity odd) function The output will stand at its defined 1-state if, and only if, an odd number (1, 3, 5, etc.) of inputs stand at their defined 1-states.	
6 400-30/1		 Even function The output will stand at its defined 1-state if, and only if, an even number (0, 2, 4, etc.) of inputs stand at their defined 1-states.	

1) This form is not preferred for future use (see 5.1).

6.4 Complex combinative functions (*concluded*)

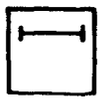
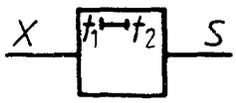
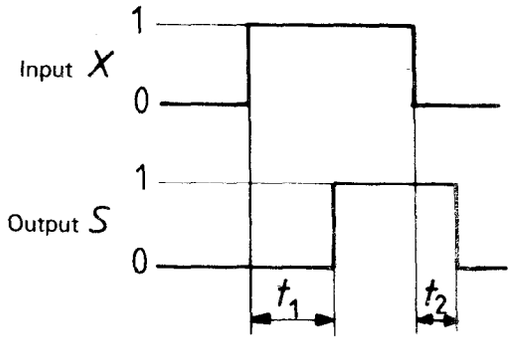
Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
6 400-35/1		 Logic identity function The output will stand at its defined 1-state if, and only if, all the inputs stand at the same static state. $S = X\,Y\,Z + \overline{X\,Y\,Z}$	

7 Delay elements

7.1 General

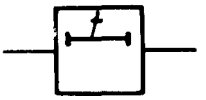
An element in which each transition at the input causes one, and only one, delayed transition at the output.

7.2 Delay elements

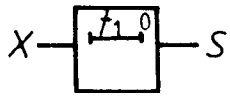
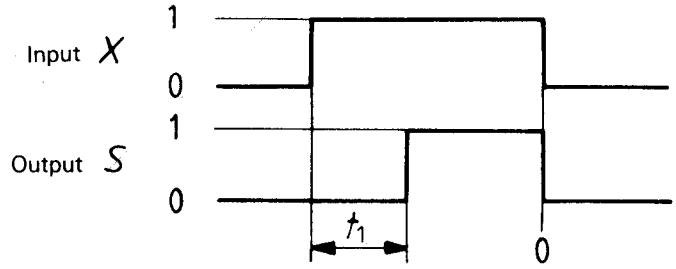
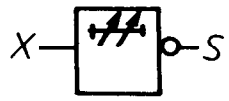
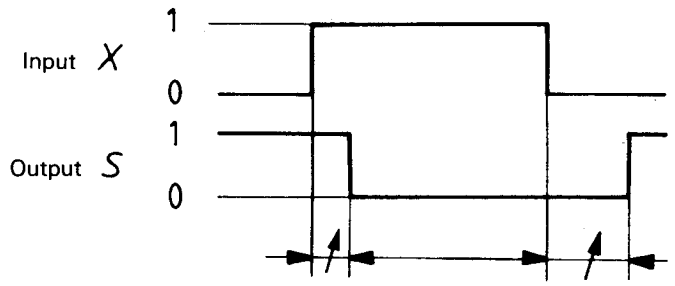
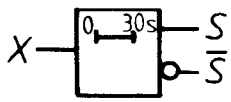
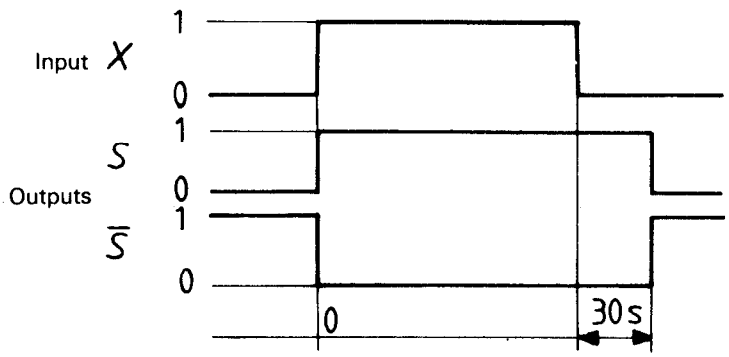
Code number	Graphical symbol	Description
7 200-05/1		Delay element General symbol
7 200-10/1		Delay element with specified delay times The transition from the 0-state to the defined 1-state at the output occurs after a delay of t_1 with reference to the same transition at the input. The transition from the defined 1-state to the 0-state at the output occurs after a delay of t_2 with reference to the same transition at the input. *Example:*  NOTE — t_1 and t_2 may be replaced by the actual delays, expressed in seconds word units or digit units, and may be placed inside or outside the outline.

1) This form is not preferred for future use (see 5.1).

7.2 Delay elements *(concluded)*

Code number	Graphical symbol	Description
7 200-15/1		If the two delays are equal, it is sufficient to insert one value.
7 200-20/1		Variable delays element
7 200-21/1		Equal variable delays element NOTE — It is possible to add the range of adjustment above the arrows.

7.3 Delay elements — Examples

Code number	Graphical symbol	Description
7 300-05/1		The transition from the 0-state to the defined 1-state occurs after a delay of t_1 and the transition from the 1-state to the 0-state is not delayed. 
7 300-10/1		Delay element with negated output for which the transition from the 0-state to the defined 1-state and the transition from the 1-state to the 0-state are delayed by two different variable delays. 
7 300-15/1		Delay element with two complementary outputs for which the transition from the 0-state to the defined 1-state is not delayed and the transition from the defined 1-state to the 0-state is delayed by 30 s. 

8 Sequential functions

8.1 Binary memory functions

8.1.1 Definition

The most common types of sequential functions are the binary memories or bistable functions.

Binary memory functions only possess two logic states characterized by the values 0 and 1 of the output variable; they often have two complementary outputs.

8.1.2 Groups of binary memory functions

The memory functions can be classified into the following two groups:

a) Group 1

Output state in relation to the application or release of both inputs simultaneously.

b) Group 2

Output state in relation to the re-establishment of supply after a temporary removal of the supply.

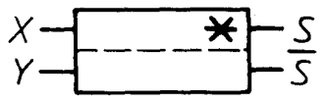
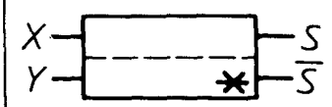
8.1.3 General symbols

Code number	Graphical symbol	Description
8 130-05/1 8 130-06/1	 	General symbol of a sequential element NOTES 1 Information flow is parallel to the dotted line. 2 Outputs placed on the same side of the dotted line are of the same type. 3 Two outputs, or groups of outputs, placed on either side of the dotted line are complementary.
8 130-10/1		This sign drawn inside the outline of the graphical symbol for the sequential elements denotes priority in the case of simultaneous signal inputs.
8 130-15/1		This sign drawn inside the outline of the graphical symbol for the sequential elements denotes holding of the set state in the case of simultaneous signal input.
8 130-20/1		This sign drawn inside the outline of the graphical symbol for the sequential elements denotes preferred set state when the momentarily removed supply is re-established in the absence of any new input.
8 130-25/1		This sign drawn inside the outline of the graphical symbol for the sequential elements denotes holding of the set state when the momentarily removed supply is re-established.
8 130-30/1	1	Logic state of inputs and outputs.
8 130-31/1	0	These signs drawn inside the outline of the graphical symbol for the sequential elements denote the logic states of outputs if necessary for particular cases (see 8.1.4.4).

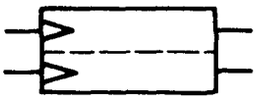
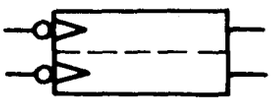
8.1.4 Binary memory functions of group 1

Examples of effect of simultaneous inputs on output states are given.

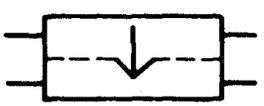
8.1.4.1 Binary memory with priority inputs

Code number	Graphical symbol	Description
8 141-05/1		Priority inscription binary memory Binary memory with two inputs (levels or pulses) with a priority for inscription signal X in case of simultaneous inputs. $S = X + S\,\overline{Y}$ $\overline{S} = (Y + \overline{S})\,\overline{X}$
8 141-10/1		Priority erasure binary memory Binary memory with two inputs (level or pulses) with a priority for erasure signal Y in case of simultaneous inputs. $S = (X + S)\,\overline{Y}$ $\overline{S} = Y + \overline{S}\,X$

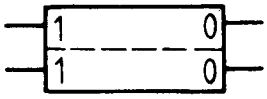
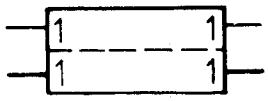
8.1.4.2 Binary memory with complemental outputs if the two inputs take simultaneously different states (binary memory with simultaneous active inputs)

Code number	Graphical symbol	Description
8 142-05/1		Binary memory with complementary outputs if the two inputs change simultaneously from the 0-state to the 1-state. The outputs always stand at complementary states. If one of the inputs takes on its defined dynamic 1-state, the output shown on the same part of the symbol takes on its defined 1-state; if both inputs take on their defined dynamic 1-states simultaneously, the outputs are complemented. If both inputs take on their 0-states, the outputs remain at their previous states.
8 142-10/1		Binary memory with complementary outputs if the two inputs change simultaneously from the 1-state to the 0-state. The outputs always stand at complementary states. If one of the inputs takes on its defined dynamic 0-state, the output shown on the same part of the symbol takes on its defined 1-state; if both inputs take on their defined dynamic 0-states simultaneously, the outputs are complemented. If both inputs take on their 1-states, the outputs remain at their previous states.

8.1.4.3 Binary memory which holds outputs in case of simultaneous signal inputs (memory with passive simultaneous inputs)

Code number	Graphical symbol	Description
8 143-05/1		Two-input binary memory which holds its previous state in the case of two simultaneous inputs. The state of memory is fixed by the nature of the last single input signal.

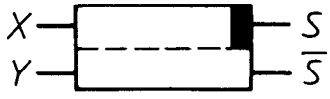
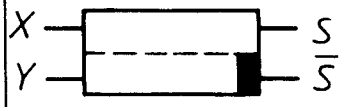
8.1.4.4 Binary memory with same state outputs in case of simultaneous signal inputs (memory with incompatible simultaneous inputs)

Code number	Graphical symbol	Description
8 144-05/1		Binary memory in which the two normally complementary outputs simultaneously assume the 0-state in the case of simultaneous inputs. NOTE – In this case, when the two input signals return simultaneously to the 0-state, the final state of the memory (output state) is undefined.
8 144-10/1		Binary memory in which the two normally complementary outputs simultaneously assume the 1-state in the case of simultaneous inputs. NOTE – In this case, when the two input signals return simultaneously to the 0 state, the final state of the memory (output state) is undefined.

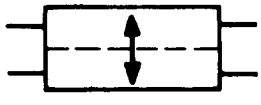
8.1.5 Binary memory functions of group 2

Examples of the effect of re-establishment of supply following temporary removal on output states are given.

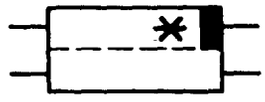
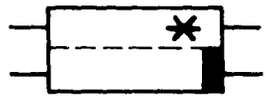
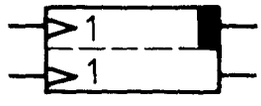
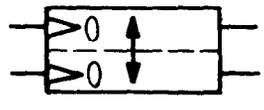
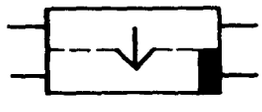
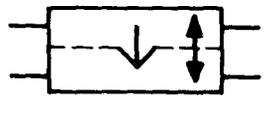
8.1.5.1 Binary memory with one priority output after re-establishment of supply following temporary removal of the supply

Code number	Graphical symbol	Description
8 151-05/1		Binary memory with priority set when the momentarily removed supply is re-established in the absence of any new inputs. $S = 1$ $S = 0$
8 151-10/1		Binary memory with priority reset when the momentarily removed supply is re-established in the absence of any new input. $S = 0$ $S = 1$

8.1.5.2 Binary memory which holds the set state of outputs after the re-establishment of supply following temporary removal of the supply

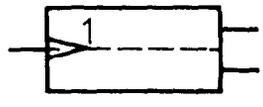
Code number	Graphical symbol	Description
8 152-05/1		Binary memory with holding of the set state when the momentarily removed supply is re-established in the absence of any new input.

8.1.6 Binary memory functions with combinations of groups 1 and 2 — Examples

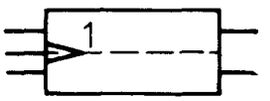
Code number	Graphical symbol	Description
8 160-05/1		Binary memory with priority set in case of simultaneous inputs, and with priority set when the momentarily removed supply is re-established.
8 160-10/1		Binary memory with priority set in case of simultaneous inputs, and with priority erasure when the momentarily removed supply is re-established.
8 160-15/1		Binary memory with complementary outputs if the two inputs change simultaneously from the 0-state to the 1-state and with priority set when the momentarily removed supply is re-established.
8 160-20/1		Binary memory with complementary outputs if the two inputs change simultaneously from the 1-state to the 0-state, and with holding of the set state when the momentarily removed supply is re-established.
8 160-25/1		Binary memory which holds its previous state in the case of two simultaneous inputs and with priority erasure when the momentarily removed supply is re-established.
8 160-30/1		Binary memory which holds its previous state in the case of two simultaneous inputs and with holding of the set state when the momentarily removed supply is re-established.

8.2 Other binary memory functions — Examples

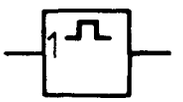
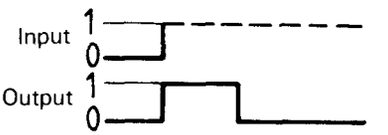
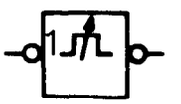
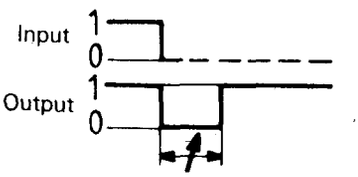
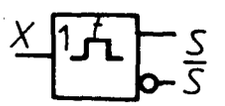
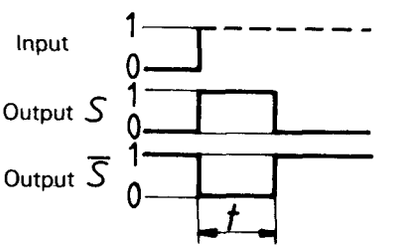
8.2.1 Other bistable binary memories

Code number	Graphical symbol	Description
8 210-05/1		Binary divider Single input memory for which the states on the outputs are complemented, if the input takes on its defined dynamic 1-state. If the input takes on its 0-state, the outputs remain at their previous states.

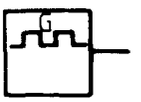
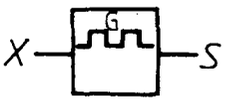
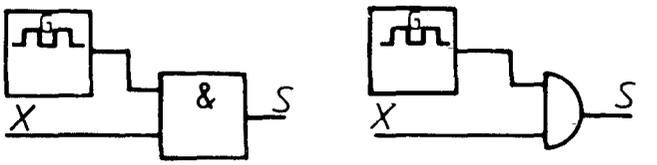
8.2.1 Other bistable binary memories *(concluded)*

Code number	Graphical symbol	Description
8 210-10/1		Binary divider with set and reset
8 210-15/1		Binary divider with holding of the set state when the momentarily removed supply is re-established.

8.2.2 Monostable element

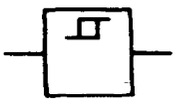
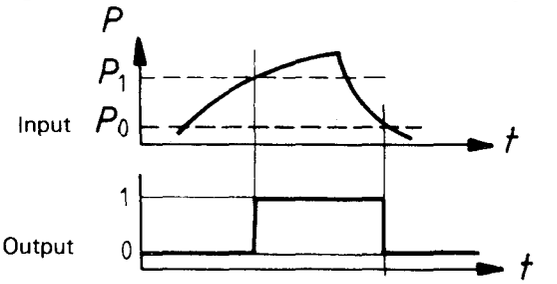
Code number	Graphical symbol	Description
8 220-05/1		Monostable stable shot The output will change to its defined 1-state only when the input changes to its defined 1-state. The output will remain in its defined 1-state for a period of time which is characteristic of the particular device, independent of the duration of the input variable.  NOTE – All other monostable elements can be defined from the above symbol with addition of negation symbol " ○ " at the input or output or at both input and output and with a possible complementary output.    

8.2.3 Astable element

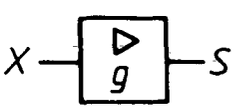
Code number	Graphical symbol	Description
8 230-05/1		Astable element (binary oscillator) General symbol NOTE — In these symbols, the letter "G" is the qualifying symbol for the generator. If the waveform is evident, these symbols may be shown without the additional symbol 
8 230-10/1		Controlled astable element Explanatory diagram 

9 Complementary symbols

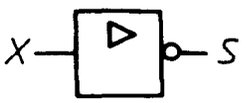
9.1 Threshold detector (Schmitt trigger)

Code number	Graphical symbol	Description
9 100-05/1		Threshold detector (Schmitt trigger) The output of a threshold detector will take up its defined 1-state only when the input signal exceeds a specific threshold value (P_1) in the direction indicated. The output remains at its defined 1-state until such time that the input signal returns below a specific threshold value (P_0) 

9.2 Amplifiers

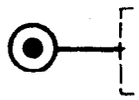
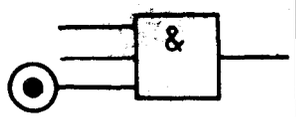
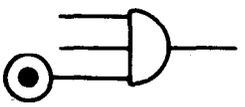
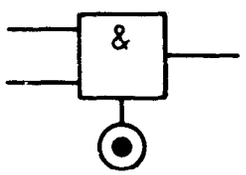
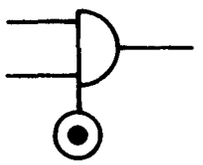
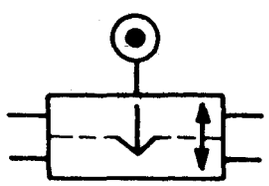
Code number	Graphical symbol	Description
9 200-05/1		Amplifier for logic diagrams (level converter) The output will stand at its defined 1-state if, and only if, the input stands at its defined 1-state. $S = X$ $g = \dfrac{\text{Value at level 1 of output}}{\text{Value at level 1 of input}}$ NOTES 1 The symbol "g" is optional. 2 The symbol "g" may be replaced by the actual value.

9.2 Amplifiers (*concluded*)

Code number	Graphical symbol	Description
9 200-10/1		Amplifier with negation indicator The output will stand at its 0-state if, and only if, the input stands at its defined 1-state. $S = \overline{X}$

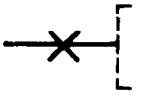
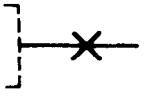
9.3 Other inputs and outputs

9.3.1 Supply input (to be used only in the case of fluid supply)

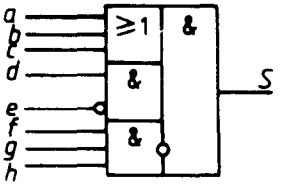
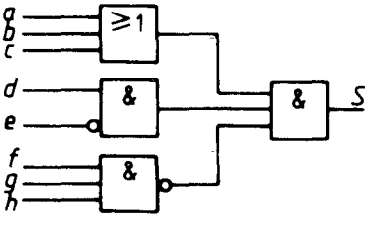
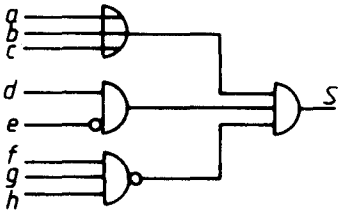
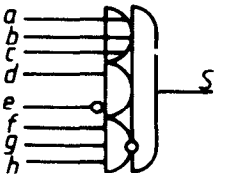
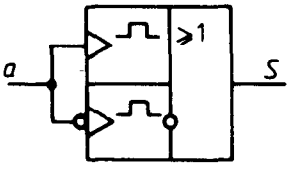
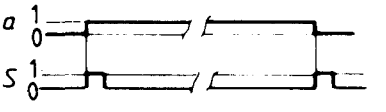
Code number	Graphical symbol	Description	Graphical symbol[1]
9 310-05/1		General symbol (see ISO 1219, item 8.1.1)	——
9 310-10/1	Form A 	AND function with supply input.	Form B 
9 310-11/1	Form A 		Form B 
9 310-15/1		Bistable binary memory with holding of the set state in the case of simultaneous inputs and in the case of re-establishement of supply conditions following temporary removal of supply, and with supply input.	——

1) This form is not preferred for future use (see 5.1).

9.3.2 Non-logic indicator line

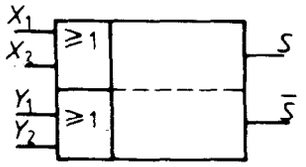
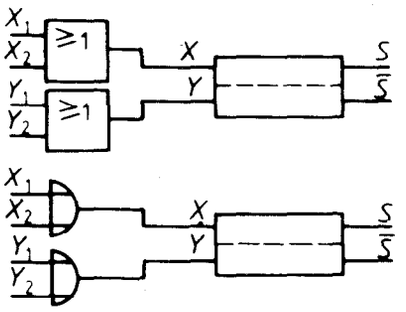
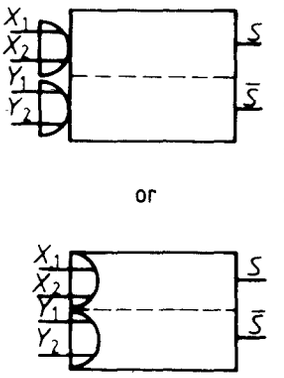
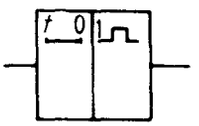
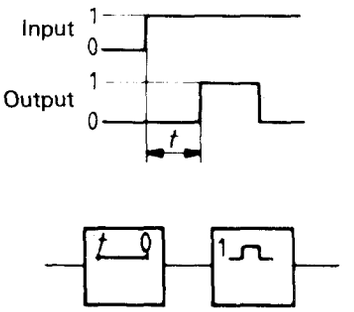
Code number	Graphical symbol	Description
9 320-05/1		Non-logic indicator input
9 320-10/1		Non-logic indicator output NOTE – The symbols 9 320-05/1 and 9 320-10/1 may be replaced by a numerical or letter value on the corresponding line.

10 Examples of symbols association (association of elementary symbols)

Code number	Graphical symbol	Description	Graphical symbol[1]
10 000-05/1	Form A 	Symbols for combinative functions *Example:* One 3-input OR function, one 2-input AND function with one negated input and one NAND function are in single connection with one 3-input AND function.   $S = (a + b + c)\, d\bar{e}\,\overline{fgh}$	Form B 
10 000-10/1		Monostable element for which the output takes the defined 1-state, during defined time, each time that the input changes state. 	—

1) Form B is not preferred for future-use (see 5,1).

10 Examples of symbols association (association of elementary symbols) (*concluded*)

Code number	Graphical symbol	Description	Graphical symbol[1]
10 000-15/1	Form A 	Binary memory with two inscription inputs and two erasure inputs connected by an OR function. 	Form B  or
10 000-20/1		Monostable element with delay 	—

1) Form B is not preferred for future use (see 5.1).

11 Identification statement (Reference to this part of ISO 5784)

Use the following statement in test reports, catalogues and sales literature when electing to comply with this part of ISO 5784:

"Symbols for binary logic and related functions in accordance with ISO 5784-1, *Fluid power systems and components — Fluid logic circuits — Part 1: Symbols for binary logic and related functions.*"

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